PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: Not Yet Assigned

Filed: December 12, 2001

For: OPTIMIZED CONTAINER STACKED CAPACITOR DRAM CELL UTILIZING SACRIFICIAL OXIDE DEPOSITION AND CHEMICAL MECHANICAL POLISHING

Examiner: Unknown

Group Art Unit: Unknown

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PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Please revise the above-identified application as follows:

IN THE SPECIFICATION:

In column 1, replace the paragraph at lines 9-11 with the following:

This is a continuation of U.S. patent application Serial No. 08/759,058, filed October 7, 1996, which is a reissue application of U.S. Patent No. 5,270,241,

issued December 14, 1993, which is a continuation of U.S. patent application Serial No. 07/850,746, filed March 13, 1992, now U.S. Patent No. 5,162,248.

In column 2, lines 10-24, please make the changes indicated below:

Also, [in] a paper submitted by T. Kaga, et al., entitled "Crown-Shaped Stacked-Capacitor Cell for 1.5-V Operation 64-Mb DRAM's," IEEE Transactions on Electron Devices. VOL. 38, NO. 2, February 1991, pp. 255-261, discusses a self-aligned stacked-capacitor cell for 64-Mb DRAM's, called a CROWN cell. The CROWN cell and its development are shown in FIGS. 7*(d)* through 7*(f)*, pp. 258 of this article. The crown shaped storage electrode is formed over word and bit lines and separated by [a] <u>an</u> oxide/nitride insulating layer with the top insulating layer being removed to form the crown shape. Capacitor dielectric film surrounds the whole surface of the storage node electrode and the top capacitor electrode is formed to complete the storage cell.

In column 3, lines 1-6, please make the changes indicated below:

is equal in height to the depth of the original contact opening. In addition, a pre-determined amount of low etch rate oxide is removed, thereby leaving oxide surrounding the [,]container, poly for both structural support and process integration for further processing which requires oxide to be left above the word lines.

In column 3, lines 29-40, please make the change indicated below:

As seen in FIG. 10, splintering effects 101 of storage node poly 93 result from a dry anisotropic etch (due to non-uniform etching of polycrystalline silicon 93) because the plasma etch reacts faster along heavily doped grain boundaries. Splinters 101 later tend to 'break off' in subsequent processing leading to contamination particulates. The trenching of the poly leads to the side-walls of the poly

container to be exposed, thus making it impossible to wet etch the oxide around the cell without translating the trenched poly horizontal portion of the etch into surrounding oxide 91 thereby leaving a ring of thin oxide around [he] the container cell.

In column 3, lines 49-54, please make the change indicated below:

FIG. 1 shows a gray scale reproduction of a SEM photograph of an array of poly containers 12 which demonstrates the uniformity and repeatability of poly containers 12 across substrate 11 that results from utilizing the process steps of the present invention discussed hereinafter.

In column 4, lines 10-15, please make the changes indicated below:

FIG. 7 is a cross-sectional view of the in-process wafer portion of FIG. 6 following blanket formations of conformal cell dielectric and polysilicon, respectively;

FIG. 8 is a cross-sectional view of a storage cell created by the present invention when integrated into a stacked capacitor fabrication process; [and]

In column 5, lines 20-53, please make the changes indicated below:

Referring now to FIG. 5, the exposed upper portions of poly 23 are removed to separate neighboring poly structures, thereby forming individual containers 51 residing in contact openings 22 and exposing underlying oxide 21. The areas of poly 23 that are removed may be accomplished by performing a poly etch selective to oxide, which could be a timed wet etch or an optimized CMP poly etch. A very significant advantage of this process flow when a CMP etch step is utilized is that the inside of the future container 51 is protected from 'slurry' contamination that is inherent in the CMP step which

proves difficult to remove in high aspect ratio storage containers (0.5μ inside diameter by 1.5μ high).

Referring now to FIG. 6, both oxides 21 and 31, which have different etch rates, are now exposed. At this point, an oxide etch is performed such that oxide 31 is completely removed from inside container 51 while a portion of oxide 21 remains at the base of container 51 and thereby providing an insulating layer between the underlying topography and subsequent layers. [A] An etch rate ratio of 2:1 or greater between (a ratio of 4:1 is preferred) oxide 31 and oxide [22] 21 provides sufficient process margin to ensure all of high etch rate oxide 31 inside container 51 is removed during the single etch step, while a portion of oxide [22] 21 remains to provide adequate insulation from subsequently formed layers.

Referring now to FIG. 7, when using this structure to form a capacitor storage node plate container 51, [and] the remaining portion of oxide 21 is coated with a capacitor cell dielectric 71. [And, finally] Finally a second conformal poly layer 72 is placed [to] onto blanket cell dielectric 71 and serves as a common capacitor cell plate to the entire array of containers 51. From this point on, the wafer is completed using conventional fabrication process steps.

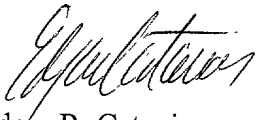
IN THE CLAIMS:

Please cancel claims 1 through 60.

REMARKS

No new matter has been added. The Applicants request entry of the foregoing amendment prior to examination of the application on the merits.

Respectfully submitted,



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